This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A method of fabricating an integrated circuit, the method comprising:

forming a barrier layer along lateral side walls and a bottom of a via aperture, the via aperture being configured to receive a via material that electrically connects a first conductive layer and a second conductive layer; and

~~providing~~ depositing a ternary copper alloy via material in the via aperture to form a via.

2. (Currently Amended) The method of claim 1, wherein the ternary copper alloy via material includes an element with a characteristic for lowering ~~resistance~~ resistivity.

3. (Currently Amended) The method of claim 2, wherein the element with a characteristic for lowering ~~resistance~~ resistivity is Zinc (Zn), Silver (Ag), or Tin (Sn).

4. (Currently Amended) The method of claim 2, wherein the element with a characteristic for lowering ~~resistance~~ resistivity is one atomic percent or less of the ternary copper alloy via material.

5. (Currently Amended) The method of claim 2, wherein the lowered ~~resistance~~ resistivity is 1.8 to 2.2 $\mu\Omega$ cm.

6. (Original) The method of claim 1, wherein the ternary copper alloy via material includes an element with a characteristic for increasing grain size.

7. (Original) The method of claim 6, wherein the element with a characteristic for increasing grain size is Calcium (Ca) or Chromium (Cr).

8. (Original) The method of claim 6, wherein the element with a characteristic for increasing grain size is one atomic percent or less of the ternary copper alloy via material.

9. (Original) The method of claim 6, wherein the increased grain size is between 0.5 and 3 μm.

10. (Original) A method of using ternary copper alloy to obtain a low resistance and large grain size interconnect or via, the method comprising:

providing a first conductive layer over an integrated circuit substrate;

providing a conformal layer section at a bottom and sides of a via aperture positioned over the first conductive layer to form a barrier separating the via aperture from the first conductive layer;

filling the via aperture with a ternary copper alloy via material to form a ternary copper alloy via; and

providing a second conductive layer over the ternary copper alloy via such that the ternary copper alloy via electrically connects the first conductive layer to the second conductive layer.

11. (Original) The method of claim 10, wherein the ternary copper alloy via material includes an element with a characteristic for lowering resistance of the ternary copper alloy via.

12. (Original) The method of claim 11, wherein the element with a characteristic for lowering resistance is Zinc (Zn), Silver (Ag), or Tin (Sn).

13. (Original) The method of claim 11, wherein the element with a characteristic for lowering resistance is one atomic percent or less of the ternary copper alloy via material.

14. (Original) The method of claim 10, wherein the ternary copper alloy via material includes an element with a characteristic for increasing grain size of the ternary copper alloy via.

15. (Original) The method of claim 14, wherein the element with a characteristic for increasing grain size is Calcium (Ca) or Chromim (Cr).

16. (Original) The method of claim 14, wherein the element with a characteristic for increasing grain size is one atomic percent or less of the ternary copper alloy via material.

17. (Original) A method of forming a via in an integrated circuit, the method comprising:

depositing a first conductive layer;

depositing an etch stop layer over the first conductive layer;

depositing an insulating layer over the etch stop layer;

forming an aperture in the insulating layer and the etch stop layer;

providing a barrier material at a bottom and sides of the aperture to form a barrier layer;

filling the aperture with a ternary copper alloy via material to form a ternary copper alloy via; and

providing a second conductive layer over the ternary copper alloy via such that the ternary copper alloy via electrically connects the first conductive layer and the second conductive layer.

18. (Original) The method of claim 17, wherein the ternary copper alloy via material includes copper (Cu), tin (Sn), and chromium (Cr).

19. (Original) The method of claim 17, wherein the ternary copper alloy via material includes copper (Cu), zinc (Zn), and chromium (Cr).

20. (Currently Amended) The method of claim 17, wherein the ternary copper alloy is CuAgCr, or CuSnCa~~, CuZrCa, or CuAgCa~~.

21. (Original) The method of claim 17, wherein the ternary copper alloy via material includes an element with a characteristic for increasing grain size of the ternary copper alloy via.

22. (Currently Amended) The method of claim 17, wherein the ternary copper alloy via includes ~~staffed~~ stuffed grain boundaries.

23. (Original) The method of claim 17, wherein the grain size of the ternary copper alloy via is 0.5 to 3 μm.